

OrCAD PCB SI

Pre- and post-layout topology exploration and signal integrity analysis

OrCAD® PCB SI delivers powerful simulation technology to help you find and address signal integrity issues throughout the design process—from conceptual circuit design in the schematic to board placement and routing. It enables pre- and post-layout topology exploration, signal analysis, and validation, allowing you to increase circuit reliability and drive known-good interconnect requirements throughout the PCB design flow to help reduce re-spins.

Overview

Addressing your signal quality challenges, inherent in today's electronic designs, is no longer relegated to just the high-end, high-speed signal integrity experts. With modern IC technology continuing to shrink, faster and faster edge rates are causing signal integrity issues to arise even in PCB designs generally not considered to be affected with "high-speed" problems or designs operating at traditionally "low" frequencies. As a result, circuit topology exploration, signal analysis, constraint development, and validation have all become essential parts of electronic product design.

OrCAD PCB SI provides powerful signal integrity tools and enables an integrated flow to explore, identify, and manage issues. Beginning in the schematic stage with pre-layout circuit simulation, you can explore and eliminate signal integrity problems early in the design process. In addition, you can follow critical nets through to the board layout with simulation to analyze and validate interconnect signal integrity during and after placement and routing.

Features

Analysis

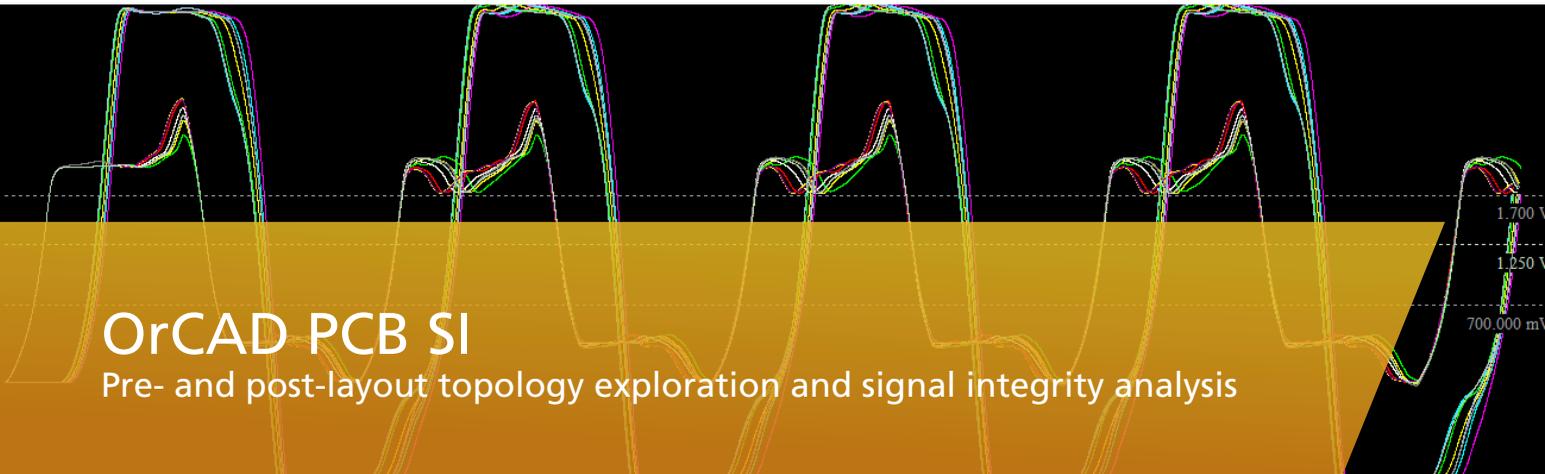
OrCAD PCB SI's simulation technology provides powerful analysis capabilities to identify a wide array of signal quality issues you might face such as reflection, overshoot and undershoot, ringing,

Highlights

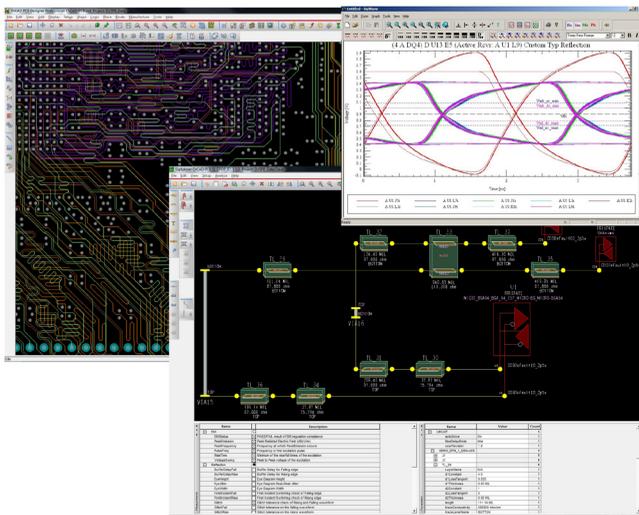
- Pre- and post-layout capabilities enable signal integrity exploration and analysis at any stage of the design cycle
- Exploration, analysis, and design of interconnect topologies help increase circuit reliability, improve circuit performance, and reduce prototypes and re-spins
- Direct integration with OrCAD PCB Editor and OrCAD Capture eliminates the need to translate design databases for simulation
- Analysis results can be converted into embedded constraints to drive known-good interconnect requirements throughout the design flow
- Support for all the latest industry-standard IBIS formats and models, generic models, and custom-built models speeds time to simulation
- Proven, scalable, signal integrity exploration and validation solution that grows as design challenges and requirements evolve

coupling, delay, and many more. The technology includes a lossy, frequency-dependent transmission-line model that accurately predicts the distributed behavior of PCB traces up to several gigahertz. An integrated electrical field solver determines the electrical characteristics of routed etch and creates electrical models of PCB vias.

Pre- and post-layout flows between schematic design and physical layout with OrCAD PCB SI enable signal integrity exploration and analysis at any stage of the design cycle. Having identified signal performance or quality issues, the OrCAD PCB



1.700 V
1.250 V
700.000 mV



OrCAD PCB SI delivers powerful simulation technology to help you find and address signal integrity issues throughout the design process

SI environment enables you to explore different what-if scenarios to determine the effects of different routing topologies, termination strategies, component values, and placement.

Pre-layout analysis

Pre-layout analysis allows you to proactively explore interconnect scenarios and simulate critical nets to minimize signal integrity problems early in the design cycle during circuit definition and schematic entry. Utilizing the tightly integrated schematic entry and signal integrity flow between OrCAD Capture and OrCAD PCB SI allows you to define optimized clock and critical signal topologies, termination components, and values, as well as routing strategies, constraints, and board stack-up requirements for layout. Once you've decided on an optimal interconnect solution, a comprehensive set of design rules and constraints is defined to drive the physical design process.

Post-layout analysis

OrCAD PCB Editor provides you with the ability to extract topologies directly from the PCB design database, enabling you to simulate critical nets to validate that the layout work matches the pre-route requirements. Topology extraction can be performed at three key stages for signal quality analysis: during part placement, after routing critical nets, and after final routing of the design. Topologies are extracted into the same SI canvas that was used to analyze the net during pre-route, and the routed signal's analysis is compared to the expected results. The extraction includes a detailed electrical representation of how the net was physically implemented, including models for trace cross-sectional characteristics, routing layers, via models, and trace lengths. If the results do not match, the routed board can be modified and the net re-analyzed.

Topology canvas and data display

OrCAD PCB SI is comprised of two primary environments: Signal Explorer and SigWave. The Signal Explorer canvas provides an electrical topology view of the physical or logical interconnect and is the simulation cockpit for analysis of high-speed or critical nets. With Signal Explorer, you begin circuit exploration with various stripline and microstrip models (lossy or lossless), drivers and receivers, and devices. Imported circuit topology, either from OrCAD Capture or OrCAD PCB Editor, is also presented in this canvas for exploration and analysis.

The SigWave canvas is the waveform viewer to display simulation results in multiple formats and modes. The oscilloscope mode allows the display of individual waveforms on and off, and provides markers for on-screen measurement.

Model Integrity

The Model Integrity module provides an editing environment within OrCAD PCB SI that allows the creation, manipulation, and validation of models quickly and easily. This module includes a model browser and syntax checker for models written in IBIS, as well as for advanced models written in DML. OrCAD PCB SI accepts device models from a variety of digital modeling formats—including support for the IBIS modeling standard—which means models created by most semiconductor manufacturers can be used. In addition, OrCAD PCB SI supports the DML modeling format, a next-generation modeling language for more complex devices. This flexible macro-modeling extension language augments IBIS and allows state-of-the-art I/O functionality to be modeled quickly and accurately.

Signal Integrity Solutions and Flows

Capture/PCB SI flow

Tightly integrated to provide a bi-directional schematic entry and signal integrity flow, OrCAD Capture and OrCAD PCB SI allow you to perform circuit topology exploration, constraint development, and signal integrity analysis from the schematic during design entry. The associated Electrical Constraint set (Electrical CSet) as well as the complete topology file is embedded in the schematic database.

PCB Editor/PCB SI flow

Routed or unrouted topologies can be extracted directly from the PCB design database, enabling you to simulate critical nets to validate that the layout work matches the pre-route requirements. Topology extraction can be performed at three key stages for signal quality analysis: during part placement, after routing critical nets, and after final routing of the design. Topologies are extracted back into the same SI canvas that was used to analyze the net during pre-route, and the routed signal's analysis is compared to the expected results. The extraction includes a detailed electrical representation of how the net was physically implemented, including models for trace cross-sectional characteristics, routing layers, via models, and trace lengths. If the results do not match, the routed board can be modified and the net re-analyzed.

Future-Proof Scalability

Unlike other signal integrity solutions, OrCAD PCB SI has the ability to grow with your evolving technology challenges and as your circuit exploration and signal integrity analysis needs change. Based on Cadence® Allegro® signal integrity technology, the OrCAD PCB SI solution provides the security of scalability to meet future challenges easily. Features and technologies are shared across the OrCAD and Allegro product lines, allowing products to be easily upgraded and expanded without the need to translate databases or libraries, learn new applications, or change use models.

For the latest product or release information, visit us at www.orcad.com or contact your local Cadence Channel Partner.

Sales, Technical Support, and Training

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